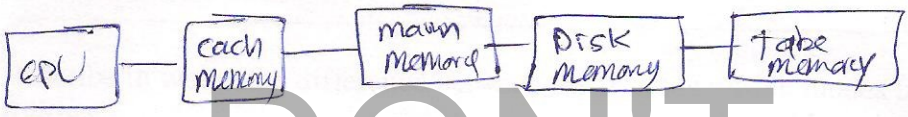
Q1- Answer the following questions (Total 38 marks)

a- What are the importances of using memory hierarchy? (2 marks)

Determine the speed and time for each memory
In addition to the cost. 2

b- Draw a block diagram of memory hierarchy used in modern computers. (4 marks)



4

c- What are the components of the datapath? (3 marks)

a. bus
b. Source, Destination
c. control signal (Read/write)

d- The RTN description of the processor state for a simple RISC computer, SRC is: (5 marks) 4

RTN	Description
PC<31---0>	Program Counter 32 bits
IR<31---0>	Instruction Register 32 bits
R[0...31]<31---0>	32 Registers each 32 bits
M[0...2^{32}-1]<7---0>	Main Memory 7bits x 2^{32}-1
Start	

e- Instruction interpretation and execution in SRC computer can be described using the abstract RTN as: (4 marks)

RTN	Description
run ∧ start → run ← 1	Set run
IR ← PC : PC ← PC+4	increment PC and move Instruction into IR

2

f- The RTN for the SPARC memory is: (6 marks)

RTN	Description
M[0...2^{32}-1]<31...0>	

2

g- The RTN of the MC68000 processor state is: (3 marks)

RTN	Description

h- Describe in words the difference between the two addressing modes in RTN as follows: (4 marks)

i- M[M[x+R[a]]]

The Address that is a combination of x and value of Ra ~~is the~~, and located in the memory, contains the address we want.

ii- M[M[x]+R[a]]

adress located in location x added with value of Ra gives the address we want

i- What are the components of ISA? (3 marks)

1- Instruction set

2- Machine memory

3- ~~RAM~~ Registers that are programmer accessable

j- We have the following information before executing the instruction: (4 marks)

1- PC =4000
2- R[1] = 100
3- R[2] = 6000
4- R[3] = 32

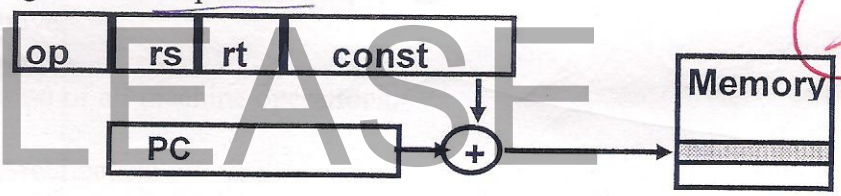
Assume we are executing the instruction **brlnz r1,r2,r3** what is the value of the registers:

1- PC = 6000
2- R[1] = 4000
3- R[2] = 6000
4- R[3] = 32

Q2- Answer the following: (12 marks)

a- Answer with F or T and correct the false statement if any. (5 marks)

1- The following addressing mode is displacement F



2- Serial buses transmit many bits simultaneously on many wires. T

3-Scientific/numerical applications like weather prediction, molecular modeling need integer arithmetic, high I/O. T

4- The address of the next address to be executed by the CPU is stored in the Instruction Register (*IR*) register. F

5- If ALU instructions only use registers for operands and result, machine type is load-store. T

b- Choose the correct answer: (7 marks)

1- The Machine State is the content of:
   a. all registers in system, accessible to programmer or not
   b. registers internal to the CPU
   c. contents of registers in the memory system
   d. None of the above

2- Choose the correct sentence that describe parallel bus:
   a. transmit one bit at a time
   b. does not provides a data path and control
   c. is a time-shared connection or multiplexer
   d. transmit many bits simultaneously on many wires

3- ---------- is the contents of all registers and machine memory, either if they are accessible to the programmer or not.
   a. Machine State
   b. Memory State
   c. Processor State
   d. None of the above

4- Cache Memory is:

a. Slower than main memory
b. Slower than hard disk
c. Faster than main memory and hard disk
d. None of the above

5- ---------- is a collection of all machine operations.

a. Instruction set
b. Instruction set Architecture
c. Resources
e. None of the above

6- Which instruction has the following interpretation?

R[8] ← PC: If (R[1] = 0 PC ← R[5])

a- brzr r5, r1
b- brlnzr r8,r5, r1.
c- brlzr r8,r5,r1
d- None of the above.

7- Following SRC instruction format can be used for:

a- lar instruction
b- ld instruction
c- la instruction
d- None of the above.

	100	1d	90	80
Sco-90	10	11	0	10-
90- Score	-10	-11	0	10

Q3- Answer the following:

a- The following C++ code determines a student grade in "ASCII" based on his/her score in a Math final exam. Using SRC instructions, convert this code to an SRC assembly program. Define all the necessary variables. (7 marks)

```
int     score;
int     grade;
if ( score >= 90 )
        grade = 65;
else if ( score >= 80)
        grade = 66;
else if ( score >= 70)
        grade = 67;
else if ( score >= 60)
        grade = 68;
else
        grade = 70;
```

```
.org 0
score .dw 1
grade .dw 1
Ld r2, grade
Ld r1, score
Sub r6, 90, score
Bgt r5, r6
```

gradeA : St r1, r2

b- Consider the following expression: (18 marks)

$$A = [(N - Z/N) / (N*M - Z) * Y]$$

i. Evaluate the following expression using:
   1. Stack machine
   2. Load/Store machine

   Assuming that A, N, M, Y, Z are stored in memory.

Stack machine		Load/Store machine

Push N
Push Z
Push N
Div
Sub
Push N
Push M
Mul
Push Z
Sub
Push Y
Mul
Pop A
	Push Z
	Push N
	Div
	Pop ABC
	Push N
	Push ABC
	Sub
	Pop P1
	Push N
	Push M
	mul
	Push Z
	Sub
	Push Y
	mul
	Push P1
	Sub
	Pop A
		Ld r1, N
		Ld r2, Z
		Ld r3, M
		Ld r4, Y
		div r10, r2, r1
		Sub r10, r1, r10
		Mul r11, r1, r3
		Sub r11, r11, r2
		mul r11, r11, r4
		Div r13, r10, r11
		St r13, A

$r_{10} = \frac{Z}{N}$

$r_{10} = N - \frac{Z}{N}$

$r_{11} = (N*M - Z)*Y$

z
1xn

7

8

ii. Assuming that the machine has 128 registers, 65 instructions and memory space equal 3 Gbytes. Calculate:

Opcode specifier = 7 | Memory specifie= 3×2^{30} | Register specifier = 2^7 |

iii. The instructions code size (in bits) that are needed to execute the expressions:

Code size (Stack machine) = for op only 1 byte
for pop, push 1 byte + 3 byte = 4 bytes
(8 x 4) + 5 = 37
Load/store codesize = 37

Code size (~~accumulator~~ machine) = 3

~~Operation 1 byte + operand 3 bytes = 4 bytes~~

Load/store operations = 1 + 3 + 3 = 7
Sub/mul/div = 1 + 3 + 3 + 3 = 10

(5 x 7) + (6 x 10) = 95
Codesize = 95 3

Q4- Answer the following:

a- Which architecture is more suitable for pipelining (CISC or RISC) (2 marks)

RISC

b- Which of the following features are RISC and which are CISC (10 Marks)

Features	RISC	CISC
Has more semantic gap between HLL and ISA		✓
Has multiple functional unit and cache		✓
Has a small of addressing mode	✓	
Has no or simple instruction pipeline	✓	
Generate compact assembly code		✓
Has fixed instruction length	✓	
Has Addressing modes that encourage memory traffic		✓
Has load/store memory access	✓	✓
Has instructions that are hard to map onto modern architectures		✓
Has a Branch delays execution	✓	

c- Consider the following machines: (13 Marks)

1- Machine A: Avaerage CPI is = 4 cycles, Working frequency= 2Ghz
2- Machine B: Avarge CPI=3 cycles, Working frequency = 2.8 Ghz

If we execute a code that has 10000 instructions on both machines; calculate:

a- Execution time for machine A

$= IC \times CPI \times T$

$= 10000 \times 4 \times 2 \times 10^{9} = 8 \times 10^{13}$

b- Execution time for machine B

$= IC \times CPI \times T$

$= 10000 \times 3 \times 2.8 \times 10^{9} = 8.4 \times 10^{13}$

c- The speed up of B machine over A machine

$$\text{Speed up} = \frac{(IC \times CPI \times T)_B}{(IC \times CPI \times T)_A} = \frac{8.4 \times 10^{13}}{8 \times 10^{13}} = 1.05$$